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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER

LEADER, WILLIAM T

ART UNIT	PAPER NUMBER
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1742

DATE MAILED: 04/04/2003

11

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/880,715

Applicant(s)

RITZDORF ET AL.

Examiner

William T. Leader

Art Unit

1742

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE three MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 6/12/2002, 10/15/2002, 02/10/2002.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 54-59 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 54-59 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ 6) ☐ Other: _____

DETAILED ACTION

Claim Objections

1. Claim 56 is objected to because of the following informalities: claim 56, as written, is dependent on claim "542". Appropriate correction of this typographical error is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35

U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35

U.S.C. 103(a).

4. Claims 54-59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dubin et al (US 5,972,192) or Poris (US 5,256,274) in view of the Lowenheim text *Electroplating* and Ameen et al (US 5,685,970).

5. The Dubin et al patent is directed to a process for electrolytically depositing copper on a semiconductor wafer. Dubin et al teach that electroplating comprises the electrodeposition of an adherent metallic coating on an electrode employing externally supplied electrons to reduce metal ions in the plating solution. A seed layer is required to carry electrical current for electroplating (column 4, lines 16-21). In carrying out the process of the Dubin et al patent, a seed layer is preliminarily deposited (column 7, lines 37-38). The Dubin et al process may be used to plate a plurality of wafers at one time, if desired, by immersing the wafers in the plating bath simultaneously (column 9, lines 16-21). One or more wafers is immersed in the bath. Following immersion, the wafer is biased negatively to make it the cathode. The applied current may be direct current for standard cathodic deposition, forward pulse current or forward-reverse pulse current where the wafer is alternately the cathode and anode. The deposition may be performed in more than one step (column 4, line 62 – column 5, line 7). As explained in the abstract,

features such as trenches and via holes on the surface of the wafer are filled by the deposition of copper.

6. The Poris et al patent is directed to a process for electrolytically depositing a metal onto a semiconductor wafer (abstract). The metal may be copper (column 3, line 3). Poris et al explain that deposition of copper occurs by the electrolysis of a copper ion-containing aqueous electrolyte. The physical laws governing this reaction were explained by Faraday in 1833. By passing an electric charge through the two electrodes immersed in the electrolyte, metal is stripped from the anode and deposited on the cathode. Positive copper ions are attracted to the negative cathode where they combine with electrons yielding neutral copper which is plated onto the electrode (column 4, lines 1-20). Prior to electrodeposition a thin diffusion barrier layer is deposited. This layer serves two functions. The first is to provide an electrically conducting layer to allow uniform metal electrodeposition across the entire wafer surface. The second is to prevent any interaction of the electrodeposited metal such as copper with the silicon or the dielectric oxide (column 6, lines 38-44 and column 11, lines 53-57). Thus, this layer serves as a seed layer for electrodeposition. In one embodiment, electrodeposition was carried out at a DC cathode current density of 5 mA/cm^2 (column 12, line 24). In choosing the anode current density, Poris notes that reference was made to printed circuit board

literature (column 8, lines 59-62). In figures 2-8, Poris illustrates that the process fills features on the top surface of the semiconductor wafer.

7. Each of the Dubin et al patent and the Poris patent teaches all of the process steps of applicant's claims except for the last step of increasing the current flow to a second current density greater than the first current density after a combined thickness of the seed and plated layers has reached a predetermined value or after a predetermined time. The secondary references show that in processes for electrodeposition over a seed layer it is known to begin plating at a low current density and to subsequently increase the current density.

8. The Lowenheim text, *Electroplating*, includes a chapter directed to Plating on Nonconductors. Lowenheim states that "To electroplate on a nonconducting medium, it is necessary that the surface of that medium be made conductive in some way" (page 417). One method disclosed by Lowenheim is to form an electrically conductive seed layer by electroless deposition. Once a nonconducting surface such as a plastic has been rendered catalytic, it is ready for the deposition of electroless copper or nickel, to be followed by conventional electroplating.

Lowenheim notes that since only the surface of the nonconductive plastic workpiece where the electroless layer has been formed is conductive, and the electroless deposit is quite thin, the conductivity of the part is not comparable to that of metallic articles where the entire thickness of the article is conductive. Lowenheim

teaches that “electroplating must be started at relatively low current densities to avoid burning at contact points” (page 423).

9. In a manner similar to Poris, Lowenheim teaches that electrochemical processes follow Faraday’s Laws which may be stated as follows:

1. The amount of chemical change produced by an electric current is proportional to the quantity of electricity that passes, and
2. The amounts of different substances liberated by a given quantity of electricity are proportional to their chemical equivalent weights.

These laws may be expressed in the form of the equation:

$$g = Iet / 96,500$$

where g = grams of substance reacting, I = current in amperes, e = chemical equivalent weight, and t = time in seconds. For an electrodeposition process, the grams of substance reacting is the amount metal deposited at the cathode. This equation indicates that there is an inverse relationship between the current applied in an electrodeposition process and the time it takes to deposit a given amount of metal. Lower current leads to longer deposition time, while higher current results in shorter deposition times. This fundamental relationship of electrodeposition provides motivation for using higher current because it allows the process to be completed more quickly, resulting in more efficient and economical operation. See pages 12-13.

10. The Ameen et al patent is cited to illustrate an application of the procedure taught by Lowenheim, and to provide additional motivation for initiating electroplating on a seed layer at a low current density followed by higher current densities. The patent is directed to a method for metallizing polymeric films by electrodeposition. The metallized films may be used in the production of circuit boards (column 1, lines 31-36). Ameen et al teach that when the non-metallic, electrically insulating substrate is a flexible polymeric sheet, the metal, such as copper, may be electrodeposited directly on a flash of metal which has been sputtered, vapor deposited, electrolessly deposited, or adhered by similar techniques on the sheet (column 1, lines 37-41). Thus, Ameen teaches the preliminary deposition of a current-carrying metallic seed layer. Conventional electrodeposition methods for copper on polymeric sheets use current densities which result in lengthy deposition times (column 2, lines 22-26). Like Lowenheim, Ameen et al recognize that the rate of metal deposition is basically dependent on the current which can be applied to the metal on the substrate, and that the current is limited by the thickness as well as the current-carrying characteristics of the metal on the substrate (column 2, lines 34-40). Ameen et al teach that the problem of long deposition time can be overcome by a method in which the current applied to the substrate is increased as the deposition process is carried out. In the invention of Ameen et al, the anode electrodes opposed to the cathodic polymeric sheet to be

plated are energized in groups. As metal is deposited onto the initial flash of metal on the substrate by the initial groups of anodes, the increased current carrying capacity of the thicker metal is utilized to allow subsequent groups of anodes to have higher energization levels. The ever increasing thickness of the metal on the substrate and its increasing current-carrying capacity, is used to increase the electrodeposition rate of metal by continually increasing the current based on the current carrying capacity of the deposited metal (column 10, lines 39 – column 11, line 3). More specifically, the first group of anodes is energized at a level which the flash metal seed layer on the substrate can handle. The first group of anodes deposits metal from the electrolytic solution onto the flash metal, thereby building up the thickness of the metal on the substrate. Eventually, each group of anodes can be energized at its desired operating level (column 11, lines 4-42). It is noted that the Ameen et al patent pertains to fabrication of circuit boards and, as stated above, that Poris mentions referring to printed circuit board literature with respect to choosing optimum anode current density. Thus, there is a recognition by Poris that prior art relating to the production of printed circuit boards is relevant to processes of metallizing semiconductor wafers.

11. The prior art of record is indicative of the level of skill of one of ordinary skill in the art. It would have been obvious at the time the invention was made to have begun the electrodeposition step of Dubin et al or Poris at a low current density and

to have increased the current density after a period of time in which the thickness and current-carrying capacity of the plated layer had grown as taught by Lowenheim and Ameen et al because burning of the initially deposited seed layer would have been avoided by using the lower current density, and the rate of deposition would have been increased by using higher current densities, thereby shortening the time needed to deposit the desired thickness of copper and performing the deposition process more efficiently.

12. Claim 54 of this application has been copied by the applicant from U. S. Patent No. 6,074,544. This claim is not patentable to the applicant for the reasons set forth above.

An interference cannot be initiated since a prerequisite for interference under 37 CFR 1.606 is that the claim be patentable to the applicant subject to a judgement in the interference.

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The Ting et al patent (US 5,969,422) discloses electroplating copper over a seed layer to form an interconnect structure on a semiconductor device, and is incorporated by Dubin et al (applied above) at column 7, lines 38-42.

The Borrione et al patent (US 5,207,883) is directed to an electrolyzer for use in an electrolysis process. At column 4, lines 3-10, Borrione et al give the formula for electrical resistance. This formula is

$$R = \rho L / A$$

where R is the resistance in micro-ohms, ρ is the resistivity in micro-ohms/centimeter, L is the length in centimeters, and A is the cross sectional area in square centimeters. This formula shows that as the cross sectional area of a conductor decreases, the resistance to current flow of the conductor increases. Thus, the resistance of a thin seed layer which would have a small cross section would be high. As metal was deposited onto the seed layer and the cross section increased, the resistance would become lower.

The Nakakoji et al patent (US 5,403,468) is directed to electroplating tin on a steel strip. As column 5, lines 36-38, Nakakoji et al indicate that the electroplating current passing through the workpiece causes resistance heating to occur. The degree of heating would depend on the amount of current and the resistance of the workpiece. As shown by formula above, the resistance is proportional to cross sectional area. Thus, an article with a smaller cross section would exhibit a greater degree of resistance heating.

The Goldberg patent (US 5,484,518) is directed to an electroplating process useful in the fabrication of printed circuit boards. Goldberg is cited for the

observation at column 8, lines 16-20, that "Theoretically, a low initial current density should be preferred with current density increased as an initial deposit is formed. This would be expected to prevent burnoff of the thin conversion coating." This recognition of accepted plating theory is the same as that taught by Lowenheim, i.e. that a low initial current density should be used in plating on a nonconductor to avoid burning the thin seed layer, and that after a period of time in which an initial deposit is formed, the current should be increased.

The Glezen et al patent is directed to a method for electroplating a substrate surface having peaks and valleys. The current density applied in an initial step may be increased if the surface roughness produced is less than the desired surface roughness (column 4, line 59 – column 5, line 6).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William T. Leader whose telephone number is 703-308-2530. The examiner can normally be reached on Mondays-Thursdays and alternate Fridays, 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Roy King, can be reached on 703-308-1146. The fax phone numbers for the organization where this application or proceeding is assigned are

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703-872-9310 for regular communications and 703-872-9311 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0661.

WL
William Leader
March 25, 2003

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